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TRANSMITTAL FORM

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Application Number	10/625,386
Filing Date	July 23, 2003
First Named Inventor	Sundeep Chauhan
Art Unit	2816
Examiner Name	Hai Ngyuen
Attorney Docket Number	STL10986

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Seagate Technology LLC
Signature	David K. Lucente
Printed name	David K. Lucente
Date	5/16/05
Reg. No.	36,202

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Reina Smith
Typed or printed name	Reina Smith
Date	05/16/2005

PATENT

Practitioner's Docket No. STL10986

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: SundeepChauhan

Application No.: 10/625,386 Group No.: 2816
Filed: 07/23/2003 Examiner: Hai Ngyuen
For: High Speed Digital Phase/Frequency Comparator For Phase Locked Loops

Mail Stop Appeal Briefs – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION--37 C.F.R. § 41.37)

1. Transmitted herewith is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on March 15, 2005.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

other than a small entity	$500.00
Appeal Brief fee due	**$500.00**

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$500.00
Extension fee (if any)	$0.00
TOTAL FEE DUE	**$500.00**

6. FEE PAYMENT

Authorization is hereby made to charge the amount of $500.00 to Deposit Account No. 19-1038.

A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 19-1038.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sundeep Chauhan	Examiner:	Hai Ngyuen
Serial No.:	10/625,386	Group Art Unit:	2816
Filed:	July 23, 2003	Docket No.:	STL10986
Title:	HIGH SPEED DIGITAL PHASE/FREQUENCEY COMPARATOR FOR PHASE LOCKED LOOPS		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

This appeal is filed in response to the final Office action mailed November 17, 2004 and the Advisory Action mailed March 8, 2005.

(1) Real party in interest

The real party in interest is Seagate Technology LLC.

(2) Related appeals and interferences

There are no related appeals or interferences.

(3) Status of Claims

As indicated in the Advisory Action, upon filing this appeal the status of the claims will be:

Claims 1-22, 25 and 26 stand rejected and are hereby appealed.

Claims 23 and 24 are objected to and are hereby appealed.

(4) Status of Amendments

An amendment after final was filed on February 15, 2005. The Advisory Action indicated that upon filing this appeal the amendment after final will not be entered.

(5) Summary of Claimed Subject Matter

Claim 1 features a phase/frequency comparator that generates a phase error responsive to a transition location signal. This is disclosed in the specification of the present invention at page 7, lines 1-23:

> N-bit parallel latch **302** latches in the outputs of N-bit tapped delay line **300** when reference clock signal **303** transitions (either from low to high or high to low, depending on the latch design). The output of N-bit parallel latch **302** is thus a snapshot of the progress of input signal **301** through N-bit tapped delay line **300** over one cycle of reference clock signal **303**. This snapshot is fed into N-bit edge detect circuit **304**, which is described in more detail in **FIG. 4**. N-bit edge detect circuit **304** outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch **302**. This signal bit may be referred to as a transition location signal.
>
> Weighted encoder **306** converts the output of N-bit edge-detect circuit **304** into a numerical phase difference value that reflects the phase difference between input signal **301** and reference signal **303**. Phase difference calculator **308** calculates the difference between the output of weighted encoder **306** and a lock point input **309**. Lock point input **309** is used to specify a particular desired phase difference between input signal **301** and reference signal **303**. The output of phase difference calculator **308** is added to the value stored in an accumulator **310**. Accumulator **310** serves as the digital counterpart to low-pass filter **108** in the analog PLL of **FIG. 1**, as an accumulator in digital signal processing acts like an integrator (which is a kind of low-pass filter) in analog signal processing. The resulting output **311** is a digital phase error signal that can be used to control a numerically controlled oscillator (NCO), as depicted in **FIG. 7**.

Claim 10 features a controllable oscillator (DDS 704 in Fig. 7) and a phase/frequency comparator (ADPFC 700 in Fig. 7). The phase/frequency comparator is coupled to the controllable oscillator such that an output of the controllable oscillator is connected in a feedback loop to an input of the phase/frequency comparator and an output of the phase/frequency comparator is connected through a forward path to a control input of the controlled oscillator. Disclosure for this is at page 10, lines 3-19, in the specification of the present invention.

The phase/frequency comparator includes a phase detecting stage, encoding circuitry coupled to the phase detecting stage and an accumulator coupled to the encoding circuitry. This is disclosed in the specification of the present invention at page 6, line 11 to page 7, line 23. Claims 2 and 4 also provide guidance as to one interpretation of those claim features.

Claim 20 features generating a snapshot of a first signal in response to receiving a second signal and mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal. These features are also disclosed in the specification of the present invention at page 6, line 11 to page 7, line 23.

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 1-9, 21 and 22 are rejected under 35 USC 112, first paragraph.

Claims 1 and 8-19 are rejected under 35 USC 112, second paragraph.

Claims 1, 2, 7, 20, 25 and 26 are rejected under 35 USC 102(e) as being anticipated by Staszewski et al.

Claims 8 and 18 are rejected under 35 USC 103(a) as being obvious over Staszewski et al. in view of Brachmann et al.

Claims 10, 11 and 16 are rejected under 35 USC 102(e) as being anticipated by Perrott et al.

Claims 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim.

(7) Argument

<u>The rejection of claims 1-9, 21 and 22 under 35 USC 112, first paragraph</u>

<u>Claims 1-9</u>

The rejection of claims 1-9 under 35 USC 112, first paragraph, is respectfully traversed. The Office Action contends "[s]ince, the specification does not enable the phase/frequency comparator having the claimed scope, i.e. it does not enable any and every means/or element for performing the recited function such as generating a phase error responsive to a transition location signal." Noticeably absent is any support for this lack-of-enablement contention, such as the USC, CFR, MPEP or case law.

To illustrate the incorrectness of that lack-of-enablement contention, a related section in the MPEP will be discussed. MPEP 2164.08(a) states:

> A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. *In re Hyatt*, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.). When claims depend on a recited property, a fact situation comparable to *Hyatt* is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor.

That MPEP section is not applicable for at least two reasons. First, claim 1 does not fall under paragraph 6 since it is not written in the means-plus-function format and has featured structure. Second, claim 1 is a comparator that generates a phase error (recited function). However, claim 1 also recites the feature "responsive to a transition location signal." That feature excludes any and every means/or element for performing the recited function of generating a phase error. Therefore, the reasoning of MPEP 2164.08(a) is not applicable.

The Federal Circuit has explained the enablement requirement. In *Chiron Corp. v. Genentech Inc.*, 70 USPQ2d 1321, 1325 (Fed. Cir. 2004), the court discussed enablement related to a continuing application's priority claim to a related, previously filed application. The court said the following:

> Moreover, the prior application must enable one of ordinary skill in the art to practice "the full scope of the claimed invention." *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993). Clarifying this principle, this court has explained: "That is not to say that the specification itself must necessarily describe how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can often fill gaps, interpolate between embodiments, and perhaps even extrapolate beyond the disclosed embodiments, depending upon the predictability of the art." *AK Steel Corp. v. Sollac*, 344 F.3d 1234, 1244 (Fed. Cir. 2003).

(Emphasis added.) Taking into account that the enabling disclosure of the specification must be commensurate in scope with the claim under consideration, the specification of the present invention enables one skilled in the art to generate a transition location signal. Furthermore, nowhere in the specification of the present invention is there any disclosure that the *structure* disclosed is necessary to the claimed invention. And the claimed invention is in a predictable art. See *In re Fisher*, 427 F.2d 833, 839 (CCPA 1970) (the scope of enablement

varies inversely with the degree of unpredictability involved.). Thus, there is no enablement violation of claim 1. Claims 2-9 are also enabled since they depend from enabled claim 1.

Claims 21 and 22

The rejection of claims 21 and 22 under 35 USC 112, first paragraph, is respectfully traversed. The Office Action contends those claims are not enabled. That is incorrect; see the specification of the present invention at page 7, lines 11-23. Also, the Office Action's statement that "based on the Applicant's arguments filed on 9/24/04 the step of calculating the phase difference (308 in instant Fig. 3) is not essential..." That statement misinterprets what was argued. The previous arguments filed on 9/24/04 stated that the Office Action failed to meet its burden of showing the elements as being essential. Without meeting that burden, the rejection was unsupported and improper.

The rejection of claims 1 and 8-19 under 35 USC 112, second paragraph

Claims 1, 8 and 9

The rejection of claims 1, 8 and 9 under 35 USC 112, second paragraph, as being incomplete for omitting essential elements is respectfully traversed.

The Court of Appeals for the Federal Circuit, in a concurring opinion, addressed in *Reiffin v. Microsoft Corp.*, 54 USPQ2d 1915 (Fed. Cir. 2000) the legality of applying such an "omitted element test." Here's what that concurring opinion said:

> The district court accepted Microsoft's proposition that the patentee must include in every claim "each and every element" that was described as "part of his invention," whether or not the element is necessary for patentability of the claim. Failure to do so, the district court held, invalidates the claims for noncompliance with the written description requirement of Section 112 Para.1. That is not a correct statement of the law. Section 112 Para.2 instructs the applicant to "distinctly claim [ ] the subject matter which the applicant regards as his invention." This does not automatically require inclusion in every claim of every element that is part of the device or its operation.
>
> It is standard for applicants to provide claims that vary in scope and in content, including some elements of a novel device or method, and omitting others. *See* Irving Kayton, 1 *Patent Practice* (6th ed.) 3.1, 3.3 (1995):

> [P]atent practitioners typically draft a series of claims approximating a spectrum of patent protection . . . . The first way in which a claim may be made narrower is by adding a limitation to it in the form of an additional element.

Claiming an invention in this manner does not raise an issue of compliance with Section 112 Para.1. Indeed, the "omitted element test" threatens this venerable practice, which is also summarized in Ernest B. Lipscomb, III, *Lipscomb's Walker on Patents* 290-91 (1985):

> [A] claim may cover an invention embracing the entire process, machine, manufacture, or composition of matter which is described in the specification, or it may cover such sub-processes or such sub-combinations of the invention as are new, useful and patentable.

See, e.g., Special Equipment Co. v. Coe, 324 U.S. 370 (1945) (reversing the rejection of a sub-combination claim directed to the previously claimed invention less one element). While the specification must of course describe the claimed invention, it is well established that the claims need not include every component that is described in the specification. *See Aro Mfg. Co. v. Convertible Top Replacement Co.*, 365 U.S. 336, 345 [128 USPQ 354] (1961) (There is "no legally recognizable or protected 'essential' element . . . in a combination patent."). The decision in *Gentry Gallery, Inc. v. Berkline Corp.*, 134 F.3d 1473, 45 USPQ2d 1498 (Fed. Cir. 1998), cited as authority by the district court, does not hold otherwise.

Id. at 1918-19. Then the concurring opinion concluded as follows:

> When the claim is supported by the patent's disclosure, is adequately distinguished from the prior art, and otherwise meets the statutory requirements of patentability, neither law nor policy requires that the claim contain all the elements described in the specification as part of the new machine or method. The district court's controversial and incorrect decision should be confronted, not ignored.

Id. at 1918-19 (emphasis added). Apparently this "omitted elements" rejection is contrary to settled law and is not viewed as having any merit. For this reason alone, this rejection is unsupported and therefore cannot stand. As such, claims 1, 8 and 9 are allowable.

In addition, this rejection uses MPEP 2172.01 that states "a claim which fails to interrelate essential elements of the invention as defined by the applicant(s) in the specification may be rejected under 35 USC 112, second paragraph." (Emphasis added.) Focusing on the emphasized portion of that quote, the present Office Action fails to provide any objective evidence that the elements listed in this rejection of claims 1, 8 and 9 are essential elements of the invention as defined by the applicant(s) in the specification. That failure means that the

Office Action has not met the burden of supporting this rejection. As this rejection is not properly supported, claims 1, 8 and 9 are definite.

Moreover, that quotation above deals with a second paragraph rejection when a claim fails to **interrelate** essential elements of the invention. Yet this rejection contends that claims 1, 8 and 9 are incomplete for **omitting** essential elements. According to MPEP 2172.01, this "omission" rejection should properly be applied under the first, not second, paragraph of §112. For this reason alone, this rejection is unsupported and incorrect.

Claims 10-19

The rejection of claims 10-19 under 35 USC 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between necessary structural connections is respectfully traversed.

First, MPEP 2172.01 states "a claim which fails to interrelate essential elements of the invention as defined by the applicant(s) in the specification may be rejected under 35 USC 112, second paragraph, for failure to point out and distinctly claim the invention." That statement in MPEP 2172.01 is not the same as the rejection statement "as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between necessary structural connections." Since that rejection statement is not supported by MPEP 2172.01, it is respectfully requested that the next Office Action provide any statute, rule or case opinion that supports that statement.

Second, "as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between necessary structural connections" is incomprehensible. It is respectfully requested that the next Office Action explain what that statement means.

Third, MPEP 2172.01 states "a claim which fails to interrelate essential elements of the invention as defined by the applicant(s) in the specification may be rejected under 35 USC 112, second paragraph." (Emphasis added.) The present Office Action fails to provide any objective evidence that the alleged "essential structural cooperative relationships of elements" and "necessary structural connections" of claim 10 are "essential elements" of the invention as defined by the applicant(s) in the specification. That failure means that the Office Action has not

met the burden of supporting this rejection. As this rejection is not properly supported, claims 10-19 are definite.

The rejection of claims 1, 2, 7, 20, 25 and 26 under 35 USC 102(e)

The rejection of claims 1, 2, 7, 20, 25 and 26 under 35 USC 102(e) as being anticipated by Staszewski et al. is respectfully traversed.

Claim 1 features "generates a phase error responsive to a transition location signal." Claim 20 features a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal.

During examination, claims are to be given their broadest reasonable interpretation consistent with the specification, and claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. See *In re American Academy of Science Tech Center*, 70 USPQ2d 1827, 1830 (Fed. Cir. 2004). (Emphasis added.)
The specification of the present invention discloses at page 7, lines 3-10, the following:

> The output of N-bit parallel latch **302** is thus a snapshot of the progress of input signal **301** through N-bit tapped delay line **300** over one cycle of reference clock signal **303**. This snapshot is fed into N-bit edge detect circuit **304**, which is described in more detail in **FIG. 4**. N-bit edge detect circuit **304** outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch **302**. This signal bit may be referred to as a transition location signal.

Thus, the specification discloses a separate meaning for a snapshot and a transition location signal. Given that difference, the Office Action is incorrect in concluding that "the snapshot can be seen as transition location signal." This error is based on the Office Action's misapplication of the fundamental rule set forth above that claims are to be given their broadest reasonable interpretation consistent with the specification. In considering that entire rule, the separate meanings attributed in the specification to a snapshot and a transition location signal show that the Office Action's conclusion that "the snapshot can be seen as transition location signal" is erroneous. Claims 1 and 20, then, are not anticipated because this applied reference does not identically show a transition location signal. Accordingly, claims 2, 7, 25 and 26 are also allowable due to their respective dependence on allowable claims 1 and 20.

The rejection of claims 8 and 18 under 35 USC 103(a)

The rejection of claims 8 and 18 under 35 USC 103(a) as being obvious over Staszewski et al. in view of Brachmann et al. is respectfully traversed. Claim 8 depend from allowable claim 1. Claim 1 is not anticipated by Staszewski et al. Brachmann et al. do not overcome the deficiency of Staszewski et al. In addition, there is no objective evidence of any suggestion in these references, either alone or taken together, that a skilled artisan would understand the missing features of claim 1 to be taught or suggested. Therefore, claim 1 is not obvious and is allowable over these two applied references. For the same reasons and due to its dependency, claim 8 is also allowable.

Claim 18 depends from claim 10. The Office Action does not apply Staszewski et al. or Brachmann et al. to claim 10. Because of that, it is unknown how Staszewski et al. and Brachmann et al. are applied to claim 18. Therefore, this rejection of claim 18 is not supported. Claim 18 is allowable.

The rejection of claims 10, 11 and 16 under 35 USC 102(e)

The rejection of claims 10, 11 and 16 under 35 USC 102(e) as being anticipated by Perrott et al. is respectfully traversed.

Claim 10 features encoding circuitry. The encoding circuitry is to be given its broadest reasonable interpretation consistent with the specification. Claim 13 recites that the encoding circuitry includes an edge detector and a weighted encoder. Without limiting the encoding circuitry of claim 10 to include both those claim 13 features, both will be discussed for this rejection.

The edge detector is disclosed in the specification at page 7, lines 7-10 as:

> N-bit edge detect circuit **304** outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch **302**. This signal bit may be referred to as a transition location signal.

The weighted encoder is disclosed in the specification at page 7, lines 11-13 as:

> Weighted encoder **306** converts the output of N-bit edge-detect circuit **304** into a numerical phase difference value that reflects the phase difference between input signal **301** and reference signal **303**.

One skilled in the art will recognize that the A/D converter in Perrott et al. is not identical to either the edge detector or the weighted encoder. Because of that deficiency in Perrott et al., claim 10 is not anticipated and is allowable. Claims 11 and 16 are also allowable due to their dependence on allowable claim 10.

The objection to claims 23 and 24

The objection to Claims 23 and 24 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim is respectfully traversed. Since claim 20 is allowable as explained above, claims 23 and 24 as they are presently are allowable.

Other matters

The objection of claims 9 and 19 under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim will be addressed, either by amendment or cancellation, upon the favorable outcome of this appeal.

The rejection of claims 2-9 under 35 USC 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements will be addressed, either by amendment or cancellation, upon the favorable outcome of this appeal.

Conclusion

Appellant maintains that present claims identify the features and benefits of the present invention clearly and concisely. The present invention as claimed is not disclosed, taught or suggested by the prior art of record or any combination thereof. Therefore, it is respectfully submitted that the appealed claims are in condition for allowance, and favorable action is respectfully requested.

Respectfully submitted,

Seagate Technology LLC
(Assignee of the Entire Interest)

5/16/05
Date

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Claims Appendix

1. (previously presented) A phase/frequency comparator that generates a phase error responsive to a transition location signal.

2. (previously presented) The apparatus of claim 7, wherein the phase detecting stage further comprises:

a tapped delay line having a plurality of outputs and configured to receive a first signal; and

a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal,

wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and

wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value

3. (original) The apparatus of claim 2, further comprising:

an accumulator coupled to the encoding circuitry,

wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error.

4. (original) The apparatus of claim 3, wherein the encoding circuitry includes:

an edge detector coupled to the parallel latch; and

a weighted encoder,

wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch; and

wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal.

5. (original) The apparatus of claim 4, wherein the encoding circuitry includes:

a phase difference calculator configured to receive a lockpoint input,

wherein the phase difference calculator calculates a signed difference between the weighted numerical value and the lockpoint input; and

wherein the signed difference is presented to the accumulator as the numerical phase difference value.

6. (original) The apparatus of claim 4, wherein the weighted numerical value is presented to the accumulator as the numerical phase difference value.

7. (previously presented) The apparatus of claim 1 further comprising: a phase detecting stage that generates a result that represents an instantaneous phase difference; and

encoding circuitry coupled to the phase detecting stage;

wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value

8. (previously presented) The apparatus of claim 1, wherein the apparatus is implemented on a single monolithic integrated circuit.

9. (original) The apparatus of claim 8, wherein the apparatus is implemented in a field-programmable gate array on the single monolithic integrated circuit.

10. (previously presented) A phase locked loop comprising:

a controllable oscillator; and

a phase/frequency comparator coupled to the controllable oscillator such that an output of the controllable oscillator is connected in a feedback loop to an input of the phase/frequency comparator and an output of the phase/frequency comparator is connected through a forward path to a control input of the controlled oscillator,

wherein the phase/frequency comparator includes:

a phase detecting stage;

encoding circuitry coupled to the phase detecting stage; and

an accumulator coupled to the encoding circuitry.

11. (original) The phase locked loop of claim 10, wherein the phase detecting stage further comprises:

a tapped delay line having a plurality of outputs and configured to receive a first signal; and

a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal,

wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and

wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value

12. (original) The phase locked loop of claim 11, further comprising:

an accumulator coupled to the encoding circuitry,

wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error.

13. (original) The phase locked loop of claim 12, wherein the encoding circuitry includes:

an edge detector coupled to the parallel latch; and

a weighted encoder,

wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch; and

wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal.

14. (original) The phase locked loop of claim 13, wherein the encoding circuitry includes:

a phase difference calculator configured to receive a lockpoint input,

wherein the phase difference calculator calculates a signed difference between the weighted numerical value and the lockpoint input; and

wherein the signed difference is presented to the accumulator as the numerical phase difference value.

15. (original) The phase locked loop of claim 13, wherein the weighted numerical value is presented to the accumulator as the numerical phase difference value.

16. (original) The phase locked loop of claim 10, wherein the forward path includes additional control circuitry.

17. (original) The phase locked loop of claim 10, wherein the controlled oscillator is a numerically controlled oscillator.

18. (previously presented) The phase locked loop of claim 10, wherein the phase locked loop is implemented on a single monolithic integrated circuit.

19. (original) The phase locked loop of claim 18, wherein the phase locked loop is implemented in a field-programmable gate array on the single monolithic integrated circuit.

20. (previously presented) A method comprising:

generating a snapshot of a first signal in response to receiving a second signal; and

mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal.

21. (original) The method of claim 20, further comprising:

combining the numerical phase difference value with a value in an accumulator to obtain a new accumulator value; and

presenting the new accumulator value as a result of a phase comparison.

22. (original) The method of claim 21, further comprising:

propagating the first signal through a tapped delay line;

latching outputs of the tapped delay line in a parallel latch in response to a transition in the second signal to obtain the snapshot of the first signal;

23. (original) The method of claim 20, further comprising:

detecting a location of an edge in the snapshot of the first signal; and

mapping the location into a weighted numerical value.

24. (original) The method of claim 23, further comprising:

comparing the weighted numerical value with a desired phase difference; and

presenting a difference between the weighted numerical value and the desired phase difference as the numerical phase difference value.

25. (original) The method of claim 20, further comprising:

controlling an output frequency of an oscillator using the result of the phase comparison.

26. (original) The method of claim 25, wherein one of the first signal and the second signal is an output of the oscillator.